IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Appl. No.:	09/590,584
Filed:	June 8, 2000
In re Patent to:	Tai A. Ly et al.
Patent No.:	5,764,951
Issued:	June 9,1998
Title:	METHODS FOR AUTOMATICALLY PIPELINING LOOPS

Supplemental Reissue Declaration
Via Electronic Filing

DECLARATION OF INVENTORS IN APPLICATION
FOR BROADENING REISSUE OF PATENT
Pursuant to 37 CFR 1.63 and 1.175

This declaration is made in application for broadening reissue of the above-identified patent.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHODS FOR AUTOMATICALLY PIPELINING LOOPS

the specification of which: (*check one*)
☐ is attached hereto; or
☒ was filed on June 8, 2000 as U.S. Reissue Application Serial No. 09/590,584.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below:

☐ by reason of a defective specification or drawing.
☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.
☒ by reason of other errors.

At least one error upon which this application for reissue is based is described as follows:

The limitation of claim 1 to methods comprising steps of parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value.

The limitation of claim 18 to systems comprising logic for parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 21 to computer program products comprising computer readable program code devices configured to cause a computer effect parsing of text descriptions including loops with delayed signal assignments having delay values and setting of latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 2 to methods wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The limitation of claim 20 to a system wherein a loop further includes a number, n, of wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include a number, n, of clock statements.

The limitation of claim 22 to computer program products wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The dependence of claim 4 upon claim 3 is in error. Claim 4 should be dependent upon claim 2.

The dependence of claim 5 upon claim 3 is in error. Claim 5 should be dependent upon claim 2.

The dependence of claim 6 upon claim 1 is in error. Claim 4 should be dependent upon claim 2.

Claim 10 includes typographical errors. Specifically, claim 10 should refer to "producer operations" and "consumer operations."

Claims 12-14 include typographical errors. Specifically, claims 12-14 should refer to "a group of access operations."

Claims 4-5, 25-26, 29-30, and 33-34 include errors. Specifically, claims 4, 25, 29, and 33 should state that "wait statements transition on Verilog "@posedge" statements." Claims 5, 26, 30, and 34 should state that "wait statements transition on Verilog "@negedge" statements."

Every error in the patent which was corrected in the present reissue application, and is not covered by the prior declaration submitted in this application, arose without any deceptive intention on the part of the applicant.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Joint Inventor	Tai A. Ly		
Inventor's Signature		Date	
Residence	US	Citizenship	Canada
Post Office Address	~~426-11 Camille Circle, San Jose, California 95134~~ 4001 PRENTICE LN, AUSTIN, TX 78746		

TAL

Full Name of Second Joint Inventor	David W. Knapp		
Inventor's Signature		Date	
Residence	US	Citizenship	US
Post Office Address	2107 North First Street, Suite 350, San Jose, California 95131		

Full Name of Third Joint Inventor	Ronald A. Miller		
Inventor's Signature		Date	
Residence	US	Citizenship	Canada
Post Office Address	210 Mariposa Avenue, Mountain View, California 94041		

Full Name of Fourth Joint Inventor	Donald B. MacMillen		
Inventor's Signature		Date	
Residence	US	Citizenship	US
Post Office Address	75 Woodridge Road, Hillsborough, California 94010		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Appl. No.:	09/590,584
Filed:	June 8, 2000
In re Patent to:	Tai A. Ly et al.
Patent No.:	5,764,951
Issued:	June 9, 1998
Title:	METHODS FOR AUTOMATICALLY PIPELINING LOOPS

Supplemental Reissue Declaration
Via Electronic Filing

DECLARATION OF INVENTORS IN APPLICATION
FOR BROADENING REISSUE OF PATENT
Pursuant to 37 CFR 1.63 and 1.175

This declaration is made in application for broadening reissue of the above-identified patent.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHODS FOR AUTOMATICALLY PIPELINING LOOPS

the specification of which: (*check one*)
☐ is attached hereto; or
☒ was filed on June 8, 2000 as U.S. Reissue Application Serial No. 09/590,584.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below:

☐ by reason of a defective specification or drawing.
☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.
☒ by reason of other errors.

At least one error upon which this application for reissue is based is described as follows:

The limitation of claim 1 to methods comprising steps of parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value.

The limitation of claim 18 to systems comprising logic for parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 21 to computer program products comprising computer readable program code devices configured to cause a computer effect parsing of text descriptions including loops with delayed signal assignments having delay values and setting of latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 2 to methods wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The limitation of claim 20 to a system wherein a loop further includes a number, n, of wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include a number, n, of clock statements.

The limitation of claim 22 to computer program products wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The dependence of claim 4 upon claim 3 is in error. Claim 4 should be dependent upon claim 2.

The dependence of claim 5 upon claim 3 is in error. Claim 5 should be dependent upon claim 2.

The dependence of claim 6 upon claim 1 is in error. Claim 4 should be dependent upon claim 2.

Claim 10 includes typographical errors. Specifically, claim 10 should refer to "producer operations" and "consumer operations."

Claims 12-14 include typographical errors. Specifically, claims 12-14 should refer to "a group of access operations."

Claims 4-5, 25-26, 29-30, and 33-34 include errors. Specifically, claims 4, 25, 29, and 33 should state that "wait statements transition on Verilog "@posedge" statements." Claims 5, 26, 30, and 34 should state that "wait statements transition on Verilog "@negedge" statements."

Every error in the patent which was corrected in the present reissue application, and is not covered by the prior declaration submitted in this application, arose without any deceptive intention on the part of the applicant.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Joint Inventor	Tai A. Ly		
Inventor's Signature		Date	
Residence	US	Citizenship	Canada
Post Office Address	426-11 Camille Circle, San Jose, California 95134		

Full Name of Second Joint Inventor	David W. Knapp		
Inventor's Signature		Date	
Residence	US	Citizenship	US
Post Office Address	2107 North First Street, Suite 350, San Jose, California 95131		

Full Name of Third Joint Inventor	Ronald A. Miller		
Inventor's Signature		Date	Nov 26, 2008
Residence	US	Citizenship	Canada
Post Office Address	675 7th Street, Lake Oswego, OR 97034		

Full Name of Fourth Joint Inventor	Donald B. MacMillen		
Inventor's Signature		Date	
Residence	US	Citizenship	US
Post Office Address	75 Woodridge Road, Hillsborough, California 94010		

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Appl. No.:	09/590,584
Filed:	June 8, 2000
In re Patent to:	Tai A. Ly et al.
Patent No.:	5,764,951
Issued:	June 9,1998
Title:	METHODS FOR AUTOMATICALLY PIPELINING LOOPS

Supplemental Reissue Declaration
Via Electronic Filing

DECLARATION OF INVENTORS IN APPLICATION
FOR BROADENING REISSUE OF PATENT
Pursuant to 37 CFR 1.63 and 1.175

This declaration is made in application for broadening reissue of the above-identified patent.

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHODS FOR AUTOMATICALLY PIPELINING LOOPS

the specification of which: (*check one*)
☐ is attached hereto; or
☒ was filed on June 8, 2000 as U.S. Reissue Application Serial No. 09/590,584.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below:

☐ by reason of a defective specification or drawing.
☒ by reason of the patentee claiming more or less than he had the right to claim in the patent.
☒ by reason of other errors.

At least one error upon which this application for reissue is based is described as follows:

The limitation of claim 1 to methods comprising steps of parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value.

The limitation of claim 18 to systems comprising logic for parsing text descriptions including loops with delayed signal assignments having delay values and setting latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 21 to computer program products comprising computer readable program code devices configured to cause a computer effect parsing of text descriptions including loops with delayed signal assignments having delay values and setting of latencies of pipelines equal to said delay values is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, the loop can include N wait statements or N clock statements instead of a delayed signal assignment having a delay value

The limitation of claim 2 to methods wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The limitation of claim 20 to a system wherein a loop further includes a number, n, of wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include a number, n, of clock statements.

The limitation of claim 22 to computer program products wherein a loop further includes N wait statements is more limiting than necessary, and resulted in the patentee claiming less than he had a right to claim. Specifically, said loops can further include N clock statements.

The dependence of claim 4 upon claim 3 is in error. Claim 4 should be dependent upon claim 2.

The dependence of claim 5 upon claim 3 is in error. Claim 5 should be dependent upon claim 2.

BY:----------

The dependence of claim 6 upon claim 1 is in error. Claim 4 should be dependent upon claim 2.

Claim 10 includes typographical errors. Specifically, claim 10 should refer to "producer operations" and "consumer operations."

Claims 12-14 include typographical errors. Specifically, claims 12-14 should refer to "a group of access operations."

Claims 4-5, 25-26, 29-30, and 33-34 include errors. Specifically, claims 4, 25, 29, and 33 should state that "wait statements transition on Verilog "@posedge" statements." Claims 5, 26, 30, and 34 should state that "wait statements transition on Verilog "@negedge" statements."

Every error in the patent which was corrected in the present reissue application, and is not covered by the prior declaration submitted in this application, arose without any deceptive intention on the part of the applicant.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Joint Inventor	Tai A. Ly		
Inventor's Signature		Date	
Residence	US	Citizenship	Canada
Post Office Address	426-11 Camille Circle, San Jose, California 95134		

Full Name of Second Joint Inventor	David W. Knapp		
Inventor's Signature		Date	
Residence	US	Citizenship	US
Post Office Address	2107 North First Street, Suite 350, San Jose, California 95131		

Full Name of Third Joint Inventor	Ronald A. Miller		
Inventor's Signature		Date	
Residence	US	Citizenship	Canada
Post Office Address	210 Mariposa Avenue, Mountain View, California 94041		

Full Name of Fourth Joint Inventor	Donald B. MacMillen		
Inventor's Signature	Donald B. MacMillen	Date	19 Feb 2008
Residence	US	Citizenship	US
Post Office Address	75 Woodridge Road, Hillsborough, California 94010		